> Generating. in the circuit, region bits representing a location each of the first, the second and third vertices with respect to a tile being rendered (See Abstract, Fig 1, col 1 line 5-40, col 1 line 67-col 3 line 62, col 11 line 8-38, col 14 line 16-col 15 line 34)
>
> Outputting coordinate data to a rasterizer, the coordinate data representing [an initial rasterization starting point estimate] based on the region bits. (See Abstract, Fig 1, col. 1 line 5-40, col 1 line 67-col 3 line 62. col 11 line 8-38, col 14 line 16-col 15 line 34)
>
> Wakasu does not specifically disclose that the estimated rasterization starting method of finding the starting raster points point. However, Duluk, Jr teaches that the method of finding the starting raster points by using the vertices of the polygon (See col 11 line 33-col 14 line 30) The motivation would have been to decreasing a substantial time of the rasterization- (See col 1 line 49-52 in Wakasu) Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Duluk, Jr into the teaching of Wakasu.

Applicants respectfully traverse the Examiner's rejection of Claim 1. Contrary to the Examiner's assertion, Applicants cannot find in Wakasu any disclosure or suggestion of Claim 1's "region bits representing a location each of the first, second, and third vertices with respect to a tile being rendered." In additional to allowing estimation of the initial rasterizing starting point, as recited in Claim 1, such region bits allow trivial discard of triangles which lie completely outside of a tile, by simply comparing the region bit patterns against known cases (See, for example, Applicants' Specification, beginning at page 9, line 16 to page 10, line 11). In contrast, Wakasu's algorithm (e.g., discussed in Wakasu's col. 14, line 16 to col. 16, line 25) discloses or suggests neither region bits nor the notion of a tile. If the Examiner disagrees, the Examiner is respectfully requested to point out by column and line numbers the specific section in Wakasu that the Examiner is relying upon to teach Applicants' region bits. Thus, Applicants respectfully submit that Claim 1 is allowable over the combined teachings of Wakasu and Duluk. Claim 4, which likewise recites "region bits," are believed allowable over Wakasu and Duluk.

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With respect to Claim 2, the Examiner states:

> Regarding claim 2, Wakasu discloses that generating, in the circuit, an [orientation bit] representing an orientationof a line connecting the first and second vertices with a line connecting the first and third vertices. (See Abstract, Fig 1, col 1 line 5-40, col 1 line 67-col 3 line 62. col 11 line 8-38, col 14 line 16-col 15 line 34)
>
> The combination of Wakasu and Duluk, Jr do not explicitly disclose that representation of orientation bit. However, Examiner take Official Notice that orientation bit is a well known art to represent the x-y coordinate data of each vertex in different coordinate system with easy manner. Therefore, it would have been obvious to one skilled in the art to have orientation bit into the teaching of Wakasu.

Applicants respectfully traverse the Examiner's rejection of Claim 2. On page 8, at lines 32-35, Applicants teach:

> An orientation circuit 130 generates a bit CW having a value 1 only if the line ("line 0'2'") connecting vertex 0' and 2' is oriented clockwise from the line ("line 0'1'") connecting vertex 0' and 1'.

Thus, the orientation bit recited in Applicants' Claim 2 relates to the relative positions of a first side of the triangle relative to a second side of the triangle. Clearly, such an orientation bit is different from the orientation bit that is "well known art to represent the x-y coordinate data of each vertex in different coordinate system with easy manner," and as to which the Examiner took Official Notice. Accordingly, Applicants respectfully submit that the Examiner's Official Notice, in combination of Wakasu and Duluk neither discloses nor suggests Applicants' Claim 2. Accordingly, Applicants respectfully submit that Claim 2, and likewise Claim 5 (which also recite an orientation bit) also, are allowable over Wakasu and Duluk.

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Claims 3 and 6, depending from Claims 2 and 4 respectively, are allowable over Wakasu and Duluk for the reasons stated above.

Thus, all claims (i.e., Claims 1-6) are allowable, and their allowance respectfully requested. If the Examiner has any question regarding the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants at 408-453-9200.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on February 7, 2001.

Attorney for Applicant(s) — Date of Signature: 2/7/2001

Respectfully submitted,

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